NOTE

DATE: March 2009

TO: Aerospace customers

SUBJECT: **MH1RT ARAM Compiler**

On a recent MH1 composite array, it has been observed wrong data coming from embedded RAM. After analysis, ATMEL found a potential risk when the RAM coming from the ARAM/MH1RT Compiler is accessed in an asynchronous way.

This phenomenon is observed in very specific conditions:

- when addresses change in the setup / hold window during a READ access, i.e when a timing violation occurs between addresses and the memory enable,
- and after changes of specific addresses according to the size and format of the memory

In case of composite array, currently, ATMEL issues to the customer, 2 RTL models, one Verilog and one VHDL.

In such case of timing violation, today the Verilog model invalidates (set to X) the entire memory plan while the VHDL model invalidates only the Data output during this violation.

As, even if ATMEL delivered full tested parts, due to the synchronous way mandatory on the tester side, this phenomenon could be hidden and could affect the delivered parts, one asks to the customers using the embedded RAM on their application board in an asynchronous way, to contact ATMEL.

Corrective action

It was decided, whatever is the size and the type of the hard block (SRAM/TPRAM/DPRAM) to invalidate in the RTL models (VHDL and Verilog) the entire memory plan when such event occurs (memory access during the set-up/hold window) to be more realistic and safe.

These models already exist for Verilog, for VHDL are available on specific request and will be available in the next Design Kit release.