Radiation-Tolerant 8-bit AVR Microcontroller

ATmegaS128

DATASHEET PRELIMINARY SUMMARY

Introduction

The Atmel® ATmegaS128 is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmegaS128 achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Features

- High-performance, Low-power Atmel AVR 8-bit Microcontroller
- Advanced RISC Architecture
  - 133 Powerful Instructions - Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers + Peripheral Control Registers
  - Fully Static Operation
  - Up to 8MIPS Throughput at 8MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 128KBytes of In-System Self-programmable Flash program memory
  - 4KBytes EEPROM
  - 4KBytes Internal SRAM
  - Write/Erase cycles: *To Be Defined after characterization*
  - Data retention: *To Be Defined after characterization*
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Up to 64 KBytes Optional External Memory Space (ATmega103 compatibility mode)
  - Programming Lock for Software Security
  - SPI Interface for In-System Programming
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard

  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - Two Expanded 16-bit Timer/Counters with Separate Prescaler, Compare Mode and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Two 8-bit PWM Channels
  - 6 PWM Channels with Programmable Resolution from 2 to 16 Bits
  - Output Compare Modulator
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Dual Programmable Serial USARTs
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Software Selectable Clock Frequency
  - ATmega103 Compatibility Mode Selected by a Fuse
  - Global Pull-up Disable
- I/O and Packages
  - 53 Programmable I/O Lines
  - 64-lead Ceramic Quad Flat Package (CQFP)
- Operating range
  - Voltage : 3V to 3.6V
  - Temperature : -55°C to +125°C
- Speed Grades
  - 0 - 8MHz
- Radiation Tolerance
  - No Single Event Latch-up below a LET threshold of 62.5 MeV/mg/cm^2@125°C
  - Tested up to a Total Ionizing Dose of 30 krads(Si) according to MIL-STD-883 Method 1019
- ESD better than : *To Be Defined after characterization*
- Mass : 4.8 g

Table of Contents

1. Description

The Atmel AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmegaS128 provides the following features: 128Kbytes of In-System Programmable Flash with Read-While-Write capabilities (1), 4Kbytes EEPROM, 4Kbytes SRAM, 53 general purpose I/O lines, 32 general purpose working registers, one Real Time Counter (RTC), 4 flexible Timer/Counters with compare modes and PWM, 2 USARTs, one byte oriented Two-wire Serial Interface, one 8-channel, 10-bit ADC with optional differential input stage with programmable gain, one programmable Watchdog Timer with Internal Oscillator, one SPI serial port, one IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and 6 software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to keep operating. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer keeps running, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer keeps running.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read- While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmegaS128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications in Space Environment.

The ATmegaS128 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Note: 1. read-only capabilities during space flights

2. Space Quality Grade

The ATmegaS128 has been developed and manufactured according to the most stringent requirements of ISO-TS-16949 grade 1 and MIL-PRF-38535 International Standards and Atmel AEQA0236 specification. This datasheet provides limit values extracted from the results of extensive characterization (versus temperature and voltage). The quality and reliability of the ATmegaS128 have been verified during regular product qualification in compliance with MIL-PRF-38535 and MIL-STD-883 standards.

3. Configuration Summary

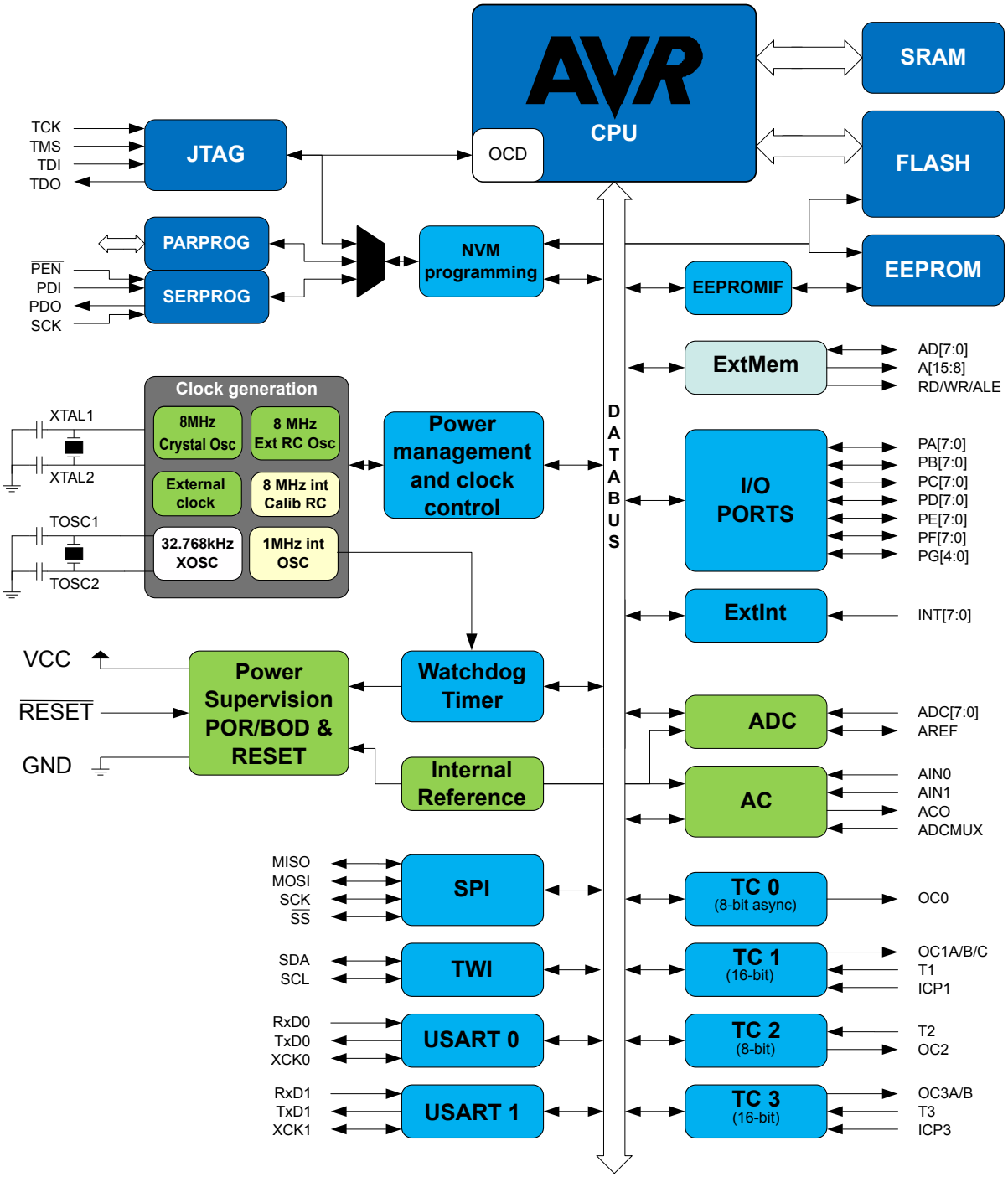
Features	ATmegaS128
Pin count	64
Flash (KB)	128
SRAM (KB)	4
EEPROM (KB)	4
External Memory (KB)	64
General Purpose I/O pins	53
SPI	1
TWI (I^2C)	1
USART	2
ADC	10-bit, up to 76.9ksps (15ksps at max resolution)
ADC channels	8
AC propagation delay	Typ 400ns
8-bit Timer/Counters	2
16-bit Timer/Counters	2
PWM channels	6
RC Oscillator	+/-3%
Operating voltage	3.0-3.6V
Max operating frequency	8 MHz
Temperature range	-55°C to 125°C
JTAG	Yes

4. Ordering Information

Ordering Code	Speed (MHz)	Power Supply	Package	Flow
ATmegaS128-ZC-E	8 MHz	3.0-3.6V	CQFP64	Engineering Samples
ATmegaS128-ZC-MQ				QML-Q equivalent
ATmegaS128-ZC-SV				QML-V equivalent

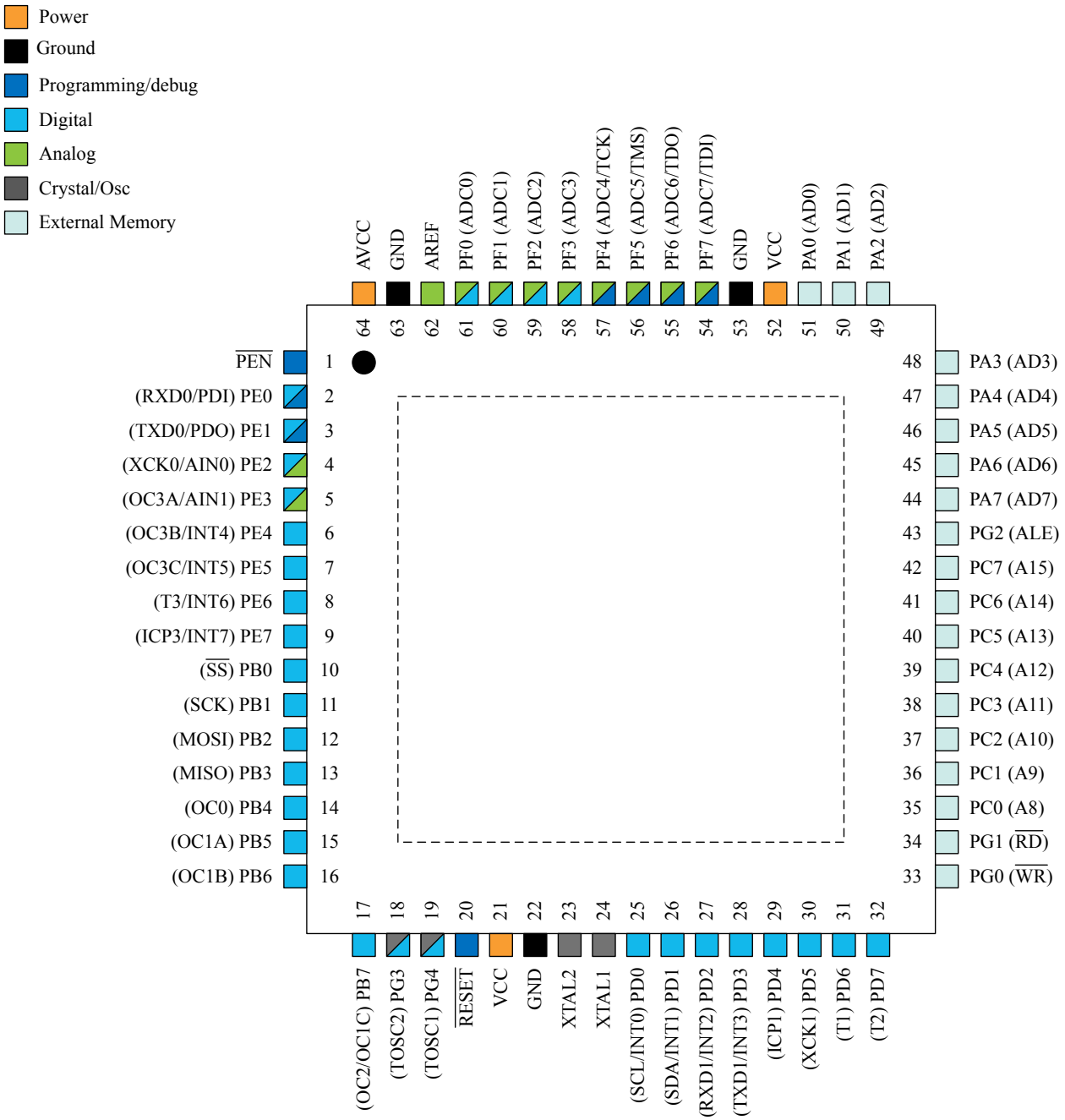
5. Block Diagram

Figure 5-1 Block Diagram



6. Pin Configurations

Figure 6-1 Pinout ATmegaS128



6.1. Pin Descriptions

6.1.1. V_{CC}

Digital supply voltage.

6.1.2. GND

Ground.

6.1.3. Port A (PA7:PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tristated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmegaS128 as listed in *Alternate Functions of Port A*.

6.1.4. Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tristated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmegaS128 as listed in *Alternate Functions of Port B*.

6.1.5. Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tristated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmegaS128 as listed in *Alternate Functions of Port C*. In ATmega103 compatibility mode, Port C is output only, and the port C pins are not tri-stated when a reset condition becomes active.

Note: The Atmel AVR ATmegaS128 is by default shipped in ATmega103 compatibility mode. Thus, if the parts are not programmed before they are put on the PCB, PORTC will be output during first power up, and until the ATmega103 compatibility mode is disabled.

6.1.6. Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tristated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmegaS128 as listed in *Alternate Functions of Port D*.

6.1.7. Port E (PE7:PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tristated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmegaS128 as listed in *Alternate Functions of Port E*.

6.1.8. Port F (PF7:PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive

characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a Reset occurs.

The TDO pin is tri-stated unless TAP states that shift out data are entered.

Port F also serves the functions of the JTAG interface.

In ATmega103 compatibility mode, Port F is an input Port only.

6.1.9. Port G (PG4:PG0)

Port G is a 5-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tristated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features.

The port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

In Atmel AVR ATmega103 compatibility mode, these pins only serves as strobes signals to the external memory as well as input to the 32kHz Oscillator, and the pins are initialized to PG0 = 1, PG1 = 1, and PG2 = 0 asynchronously when a reset condition becomes active, even if the clock is not running. PG3 and PG4 are oscillator pins.

6.1.10. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in *System and Reset Characteristics*. Shorter pulses are not guaranteed to generate a reset.

6.1.11. XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

6.1.12. XTAL2

Output from the inverting Oscillator amplifier.

6.1.13. AV_{CC}

AV_{CC} is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

6.1.14. AREF

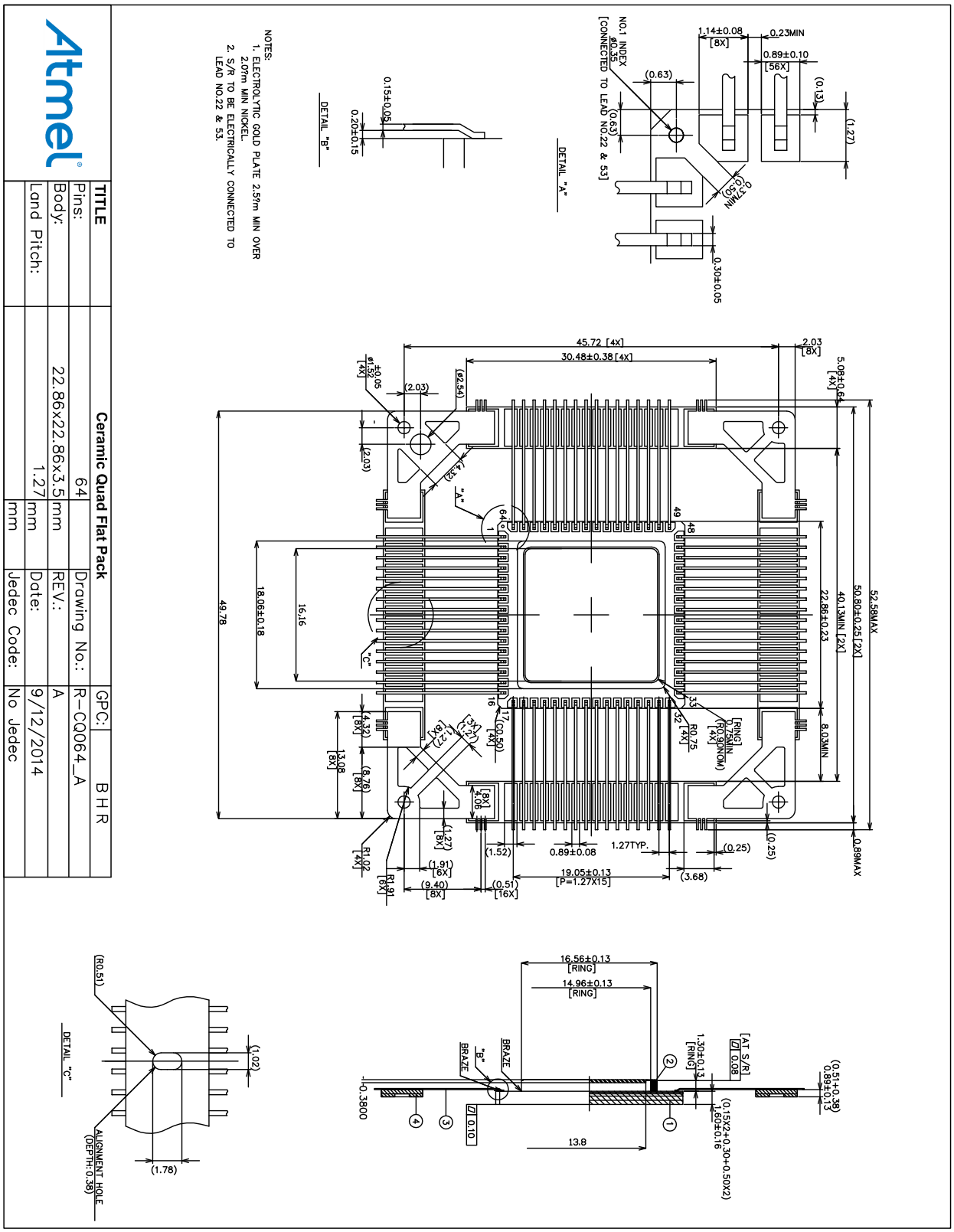
AREF is the analog reference pin for the A/D Converter.

6.1.15. PEN

PEN is a programming enable pin for the SPI Serial Programming mode, and is internally pulled high. By holding this pin low during a Power-on Reset, the device will enter the SPI Serial Programming mode. $\overline{\text{PEN}}$ has no function during normal operation.

7. Packaging Information

7.1. CQFP64



8. Errata

The revision letter in this section refers to the revision of the ATmegaS128 device.

8.1. ATmegaS128 Rev. U

- First Analog Comparator conversion may be delayed
- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Stabilizing time needed when changing XDIV Register
- Stabilizing time needed when changing OSCCAL Register
- IDCODE masks data from TDI input
- Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request

1. **First Analog Comparator conversion may be delayed**
   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix/Workaround

   When the device has been powered or reset, disable then enable the Analog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**
   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

3. **Stabilizing time needed when changing XDIV Register**
   After increasing the source clock frequency more than 2% with settings in the XDIV register, the device may execute some of the subsequent instructions incorrectly.

   Problem Fix/Workaround

   The NOP instruction will always be executed correctly also right after a frequency change. Thus, the next 8 instructions after the change should be NOP instructions. To ensure this, follow this procedure:

   3.1. Clear the I bit in the SREG Register.
   3.2. Set the new pre-scaling factor in XDIV register.
   3.3. Execute 8 NOP instructions
   3.4. Set the I bit in SREG

   This will ensure that all subsequent instructions will execute correctly.

   Assembly Code Example:

```
CLI                     ; clear global interrupt enable
OUT   XDIV, temp        ; set new prescale value
NOP                     ; no operation
NOP                     ; no operation
NOP                     ; no operation
```

```
NOP                     ; no operation
NOP                     ; no operation
NOP                     ; no operation
NOP                     ; no operation
NOP                     ; no operation
SEI                     ; set global interrupt enable
```

4. **Stabilizing time needed when changing OSCCAL Register**
   After increasing the source clock frequency more than 2% with settings in the OSCCAL register, the device may execute some of the subsequent instructions incorrectly.

   Problem Fix/Workaround

   The behavior follows errata number 3., and the same Fix / Workaround is applicable on this errata.

5. **IDCODE masks data from TDI input**
   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix/Workaround

   - If ATmegaS128 is the only device in the scan chain, the problem is not visible.
   - Select the Device ID Register of the ATmegaS128 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmegaS128 while reading the Device ID Registers of preceding devices of the boundary scan chain.
   - If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmegaS128 must be the first device in the chain.

6. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**
   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix/Workaround

   Always use OUT or SBI to set EERE in EECR.

9. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

9.1. Rev. 41036BS – 10/15

1. Complete document update based on the ATmega128A document "Atmel-8151JS-8-bit AVR Microcontroller_datasheet _Summary-09/2015

9.2. Rev. 41036AS – 02/14

1. Initial revision. (Based on the ATmega128A industrial version document "8151HS-AVR-02/11)

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